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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/191,629	TRAN ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-38,40-46,48-52 and 57-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *48--52* is/are allowed.

6)☒ Claim(s) *1-6,8-38,40-43,46,57-61* is/are rejected.

7)☒ Claim(s) *44 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim **57 is** rejected under 35 U.S.C. 102(e) as being anticipated by Admitted Prior Art (APA, FIG.1).

Considering claim **57**, APA discloses all claimed subject matter, note;

a) the claimed digital television/local bus interface logic for passing decoded digital television data is met by Core Logic 10, APA, FIG.1.

b) the claimed a graphics controller for receiving the decoded digital television data over a local bus from the digital television/local bus interface logic is met by graphics controller 14, APA,FIG.1.

c) the claimed a display device for receiving the decoded digital television data from the graphics controller is met by Display Screen 34, (APA,FIG.1).

3. Claims **57-61** are rejected under 35 U.S.C. 102(e) as being anticipated by **Johnson**, U.S. Pat. No. 6,330,038.

Considering claim **57**, Johnson discloses all claimed subject matter, note;

a) the claimed digital television/local bus interface logic for passing decoded digital television data is met by video port 150, FIG.4, where decoded and analog to digital converted digital signals are passed to the graphics controller 154.

b) the claimed a graphics controller for receiving the decoded digital television data over a local bus from the digital television/local bus interface logic is met by graphics controller 154, FIG.4, the local bus being inherent in the system.

c) the claimed a display device for receiving the decoded digital television data from the graphics controller is met by Monitor 32 via VGA to Monitor interface 158.

Considering claim **58,** the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus is met by bus 108, Fig.3;

Considering claim **59**, the claimed a core logic for receiving the decoded digital television data from the digital television/local bus interface logic and passing the decoded digital television data to the graphics controller is met by video port 150, Fig.4;

Considering claim **60**, the digital television decoder for providing decoded digital television data to the digital television/local bus interface logic, is met by video decoder 146, FIG.4;

Considering claim **61**, the claimed digital television tuner for providing encoded digital television data to the digital television decoder is met by the disclosure that the A/V sub system 52 comprises two TV tuners, FIG.2.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1-6,8-38 and 40-46 are** rejected under 35 U.S.C. 103(a) as being unpatentable over Dye, U.S. Patent No. **6,067,098**.

Considering claim **1**, Dye discloses the following claimed subject matter, note;

c) the claimed method of monitoring refresh of a display device coupled to the system is met by the CPU 102, fig.3.

d) the claimed method of transmitting the outgoing digital television data in the second frame buffer to the display device when a programmed position of the display device is refreshed is met by the Display Refresh List (VDRL) Engine 240 which "executes the video display refresh list". (col. 21, lines 22-25).

Except for;

a) the claimed method of storing incoming digital television data in the first frame buffer;

b) the claimed method of reading outgoing digital television data from the second frame buffer;

e) the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding (a) and (b), Dye discloses that "The IMC 140 uses techniques to improve overall system performance and user response time by use of the main system memory as a virtual graphical frame buffer and program/data storage. The IMC 140 provides a unique system level architecture that reduces data bandwidth requirements for general media input/output functions. Because the host CPU 102 is not required to move data between main memory and the graphics and audio and telephony subsystems as in conventional computers, data can reside virtually in the same subsystem as the main memory. Therefore, for media output data (audio, video, telephony) the host CPU or DMA master is not limited by external available proprietary bus bandwidth, thus improving overall system throughput." (Col. 11, lines 52-65)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to implement the system of Dye by utilizing the system memory for both incoming and outgoing television signals instead of using separate frame buffers

for storing incoming data and for storing outgoing data, so that the system as whole is made more compact and less costly.

Regarding e), Dye does not specifically disclose that the refresh rate of the incoming digital television data is **decoupled** from a refresh rate of the outgoing digital television data. However, Dye discloses that "A graphics controller (IMC) which performs pointer-based and/or display list-based video refresh operations that enable screen refresh data to be assembled on a per window or per object basis, thereby greatly increasing the performance of the graphical display...This information is used during the screen refresh to display the various windows or objects on the screen very quickly and efficiently. Thus, the video display can be updated with new video data without requiring any system bus data transfers, which are required in prior art computer system architectures. The graphics controller dynamically adjusts the display refresh list for movement of objects and changes in relative depth priority which appear on the display...Rather, in many instances, either the video data for a respective window or object is changed, or only the pointers in the display refresh list are manipulated, to affect a screen change." (see Abstract) Further, Dye discloses, "the pointer-based display list method of the present invention also allows screen refresh rate edge anti-aliasing and filtering method to be applied to video data on the fly as data is being refreshed on the screen. As discussed above, data is read from the system memory according to the current display refresh list, which is continually updated as screen changes occur." (col. 5, lines 50-55)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Dye by providing separate refresh rate for the incoming data and the transmitted data so that the displayed image is independent

of the incoming refresh rate or that the display is not influenced by the incoming data's refresh rate, and thereby provide a smoother and more reliable display system.

Considering claim **2,**

a) storing the incoming digital television data in the second frame buffer

b) reading the outgoing digital television data from the first frame buffer

c) transmitting the outgoing digital television data in the first frame buffer to the display device when the programmed position of the display device is refreshed.

Regarding claim 2, see rejection of claim 1(a),(b) and (d), respectively.

Considering claim **3,** the claimed method of detecting whether the outgoing digital television data is stored in the first frame buffer or the second frame buffer, is met by the CPU 102, fig.3;

Considering claim **4**, the claimed method of monitoring step comprising the step of monitoring a horizontal sync and a vertical sync of the display device, is met by the disclosure "The IMC 140 couples to a display device 142, such as a computer video monitor or television screen, among others. The IMC 140 generates appropriate video signals for driving display device 142. The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142. The IMC 140 also generates NTSC video signals, PAL video signals, or video signals for other analog or digital television/video formats. The IMC 140 may generate any of various types of signals for controlling a display device or video monitor. As shown, the IMC 140 preferably uses a serial control

bus, such as the I2C serial bus, for control of the display device 142." (col. 10, lines 46-58)

Considering claim **5,** the claimed wherein the outgoing digital television data transmitted to the display device comprises a frame is met by implied because video signal are transmitted to the screen as frames or fields. (see also col. 1, line 64 to col.2, line 2)

Considering claim **6**, Dye discloses all claimed subject matter, except for;
The claimed method of transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus, is met by PCI/USB busses, Fig.2A and 2B.

Considering claim 8, Dye discloses all claimed subject matter, note;

a) the claimed local bus is met by PCI/USB Fig.2A;

b) the claimed Digital television/local bus interface logic coupled to the local bus is met by Interactive Media Controller 140, fig.2A.

c) the claimed Digital television interface for receiving incoming digital TV data is met by Host I/F 202, fig. 6;

d) a local bus interface for transmitting outgoing digital television data over the local bus is met by HD_bus 207 and D_bus 2, fig.6;

g) the claimed memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer; digital television interface for receiving incoming digital television data, is met by Memory controllers 221 and 222, fig. 6;

Except for;

e) a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

f) second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding e) and f), see rejection of claim 1 (a) and (b).

Considering claim **9**, see rejection of claim 6.

Considering claim **10**, the claimed display device coupled to the local bus for receiving outgoing digital television data over the local bus is met by display 142, figs. 2A-2B.

Considering claim **11,** the claimed wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device is met by memory controllers 221 and 222, fig.6;

Considering claim **12**, the claimed wherein the memory controller stores the incoming digital television data to the *second frame buffer* and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of a display

device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device;

Regarding claim 12, see rejection of claim 1 (a) and (b).

Considering claim **13**, the claimed wherein the local bus interface monitors a refresh of display device for receiving the outgoing digital television data is met by CPU 102, fig.2;

Considering claim **14**, the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding 14, see rejection of claim 1(d).

Considering claim **15**, the digital television local bus logic further comprising: a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer, is met by the disclosure that "The high level graphical protocol used by the IMC 140 of the present invention eliminates many of the CPU reads and writes of graphical information that are required in prior art systems. Instead, a system incorporating an IMC 140 according to the present invention includes a high level graphical protocol whereby the CPU 102 instructs the IMC 140 to manipulate the data stored in the system memory 110...Rather, the IMC 140 reads the text data into the system memory 110, preferably in ASCII format, and the IMC 140 processes the text data for display output. This operation is performed under the direction of the CPU 102 through the high level graphical protocol used by the IMC 140...In current prior art systems, this operation requires either extra cost for memory in the graphical subsystem, i.e., additional video memory or VRAM, or the CPU

102 is required to move the occluded information from the graphical subsystem back into the system memory for temporary storage." (col. 13, lines 29-60)

Considering claim **16**, the claimed the digital television/local bus logic further comprising: a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

Regarding claim 16, see rejection of claim 15.

Considering claim **17**, a digital television/local bus interface logic, comprising:
a) the claimed a digital television interface for receiving incoming digital television data is met by the Host I/F 202, Fig.6;
b) the claimed a local bus interface for transmitting outgoing digital television data is met by PCI or USB, Fig. 2A;

e) the claimed a memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmitting the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device is met by the Memory controllers 221 and 222, fig. 6;

Except for;
c) the claimed a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;
d) the claimed a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding c) and d), see rejection of claim 1 (a) and (b).

Considering claim **18**, the claimed wherein the local bus interface comprises a peripheral component interconnect (PCI) interface is met by PCI, fig.2A.

Considering claim **19**, the claimed wherein the local bus interface transmits the outgoing digital television data over a local bus.

Regarding claim 19, see rejection of claim 6.

Considering claim **20,** see rejection of claim 11.
Considering claim **21,** see rejection of claim 12.
Considering claim **22,** see rejection of claim 14.
Considering claim **23,** see rejection of claim 15.
Considering claim **24,** see rejection of claim 16.

Considering claim **25,** Dye discloses the following claimed subject matter, note;
a) the claimed a first interface means for receiving incoming digital television data is met by Host I/F 202, fig. 6;

b)a second interface means for transmitting outgoing digital television data by the 194/CCIR656 video in/out, fig. 3;

e) the claimed controller means for storing the incoming digital television data to one buffer means and reading the outgoing digital television data from another buffer means is met by CPU 102, fig.3;

except for;

c) the claimed first buffer means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

d) a second buffer means for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding c) and d), see rejection of claim 1 (a) and (b).

Considering claim **26**, the claimed wherein the second interface means for transmitting the outgoing digital television data comprises a peripheral component interconnect (PCI) interface.

Regarding claim 26, see rejection of claim 6.

Considering claim **27**, the claimed the second interface means for transmitting the outgoing digital television data transmits the outgoing digital television data over a local bus is met by HD_bus 207, fig.6;

Considering claim **28**, see rejection of claim 15.

Considering claim **29**, see rejection of claim 16.

Considering claim **30**, the claimed wherein the first interface means for receiving the incoming digital television data comprises a digital television interface.

Regarding claim 30, see rejection of claim 25 (a) and (b).

Considering claim **31**, see rejection of claim 11.

Considering claim **32**, see rejection of claim 12.

Considering claim **33**, see rejection of claim 14.

Considering claim **34**, Dye discloses all claimed subject matter, note;

c) the claimed a monitoring means for monitoring refresh of a display device is met by CPU 102, fig. 3;

d) the claimed a transmitting means for transmitting the outgoing digital television data in a storing means to the display device when a programmed position of the display device is refreshed, is met by Storage FIFO 244, fig.6;

Except for;

a) the claimed first storing means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

b) a second storing means for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

e) the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding a) and b), see rejection of claim 1(a) and (b).

Regarding e), see rejection of claim 1(e).

Considering claim **35**, a means for reading the outgoing digital television data from a storing means is met by display storage FIFO 244, fig.6; (see also rejection of claim 1 (a) and (b))

Considering claim **36**, the claimed means for monitoring a horizontal sync and a vertical sync of the display device is met by the disclosure "The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142." (col. 10, lines 49-52)

Considering claim **37**, the claimed detecting means for detecting whether the outgoing digital television data is stored in the first storing means or the second storing means is met by CPU 102, FIG.3; (see col. 13, lines 29-60 and rejection of claim 34(a) and (b))

Considering claim **38**, see rejection of claim 6.

Considering claim **40**, Dye discloses the following claimed subject matter, note;

a) the claimed local bus is met by PCI/USB, Fig. 2A/2B;

b)the claimed graphics controller coupled to the local bus is met by CPU 102, Fig. 2A;

c)the claimed display device for receiving outgoing digital television data from the graphics controller is met by display 142, Fig. 2A;

d) the claimed digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed is met by Interactive Medial Controller 140 and System Memory 110, Fig. 2A;

Except for;

e) the claimed wherein the refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data;

Regarding e), see rejection of claim 1(e).

Considering claim **41**, the claimed core logic coupled between the local bus and the graphics controller is met by Bus I/F logic 202, figs. 5 and 6;

Considering claim **42**, the claimed digital television decoder for providing incoming television data to the digital television/local bus interface logic is implied in televisions system such as Dye's;

Considering claim **43**, the claimed digital television tuner for providing incoming digital television data to the digital television decoder, is implied in televisions system such as Dye's;

Considering claim **46**, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus.

Regarding claim 46, see rejection of claim 6.

Response to Arguments

Applicant's Arguments

1) Rather than finding an embodiment of every element arranged as in the claim, the Office Action picks and chooses unrelated elements from different embodiments, as shown below... The Office Action asserts that "the claimed local bus is met by PCI/USB Fig. 2A_"c' Dye does not consider either the PCI bus or the US13 bus as local busses, but rather distinguishes local busses and peripheral busses such as PCI busses, providing separate WC 140 interfaces for local and peripheral busses,.' Dye also fails to recite either the PCI bus or the USB bus of Fig. 2A as being used for transferring digital television data. Instead, Dye recites the PCI bus "maybe used for coupling to various 1/O devices, such as non-volatile storage, network interfaces devices, etc.,' which are

conventional uses for a PCI bus. Dye nowhere recites a use for the TSB bus, bzlt merely recites the IMC 140 having an interface to a US-3 bus.

2) The Office Action further asserts that "the claimed Digital television/local bus interface logic coupled to the local bus is met by the Interactive Media Controller 140, fig. 2A. "t° Fig- 2A nowhere mentions a local bus. As shown above, Dye distinguishes between local busses and PCI busses, reciting different IMC 140 interfaces for each type of bus.

3) The Office Action further asserts that "the claimed Digital television/local bus interface logic coupled to the local bus is met by Host I/F 202, fig. 6."11. Dye nowhere shows in Fig. 6 either the PCI bus or the USB bus of Fig. 2A, previously identified as the local bus, much less shows the Host I/F 202 as a local bus interface coupled to either of the PCI and USB busses. One skilled in the art would understand a "local bus interface logic coupled to the local bus" to recite an interface logic directly connected to the local bus. Dye neither shows nor describes the Host I/F' 202 as either a local bus interface nor as a coupled to a local bus. Nor does Dye show the Host VF 202 of Fig. 6 as coupled to the PCI bus or the T.ISB bus of Fig. 2A, which is not shown in Fig. 6. Nor does Dye recite the Host VF 202 as being a "digital television/local bus interface," as in Applicants' claimed subject matter. The Host IIF 202 instead connects between "the system CPU or peripheral core logic" and the "Command and Data FIFO 205." Dye nowhere recites the Host IIF 202 as handling digital television data. Rather, the Host VF

202 apparently passes display list instructions and data to the Command and Data FIFO 205.

4) The Office Action further asserts that "a local bus interface for transmitting outgoing digital television data over the local bus is met by HD_ bus 207 and D_bus 2, 6." First, one of ordinary skill in the art would not consider two separate busses as "a local bus interface." Further, Dye nowhere even shows the PCI bus or the USB bus of Fig.2A in Fig. 6, which the Office Action has previously identified as the local bus, much less recites the HD _bus 207 and the Dbus2 of Fig. 6 as being an interface to the PCI bus or the USB bus. Even further, having previously argued the Host 1!F 202 is the "digital television/local bus interface logic," the Office Action cannot reasonably assert that one of the elements comprising that logic is met by two busses that are not only not [sic] part of the Host I/F logic 202, but are not even directly connected to the Host I/F logic 202.

5) Nor does the Dbus2 of Fig. 6 transmit outgoing digital television data over the local bus. Rather, Dye's only mention of this bus indicates "the Dbus2 is connected between the Memory Controller 2.22 and the HD bus.

6) Dye fails to disclose first and second frame buffers for storing incoming digital television data and outgoing digital television data in an alternating manner... In particular, the IMC 140 uses "foreground" buffers for a current screen refresh and

"background" buffers for a subsequent screen refresh. Thus, there is no teaching or suggestion in Dye that its two FIFOs store incoming digital television data, much less storing incoming digital television data and outgoing digital television data in an alternating manner, as in Applicants' claimed subject matter. Nor is there any teaching or suggestion that the two FIFOs function as "frame buffers." Instead, Dye expressly teaches away from the use of frame buffers, stating that frame buffers present several problems. "Thus the present invention is not required to maintain, and preferably does not maintain, a single frame buffer which contains all of the video data for display on the video screen."

7) As shown in Figure 4 in Johnson, the video port 150 is only directly connected to a video decoder 146 and a graphics controller 154_ Neither the video decoder 146 nor the graphics controller 154 is a local bus. The Office Action's view of the term, "local bus interface logic" would stretch the term far beyond the broadest reasonable interpretation of the term. The Patent Office cannot reasonably contend that a video port 150 within a graphics/video system 116 coupled to a bidirectional bus 128 that is coupled to a PCI bus 108 is somehow directly connected to the PCI bus 108. Ironically, while the Office Action characterizes a "video port" as "digital television/local bus interface logic," one advantage of Applicants' disclosed embodiment digital television/local bus interface logic is eliminating the need for a video port cable between a graphics controller and a television tuner...That is, the incoming television signal itself is digital. Johnson does not disclose or teach interface logic for such a signal. In fact, Johnson plainly indicates that

the chrominance and luminance signals are analog when received by the video decoder 146, as recognized in the Office Action. 24

8) With respect to claim 1, Dye fails to disclose reading incoming digital television data in a first frame buffer. As shown above, the Command FIFO 205 does not store incoming digital television data, but stores commands and instructions for the Execution Engine 210...The only "decoupling" addressed by Dye is decoupling of data transfers between the computer system and IMC 140 using FIFO buffers 204 and 206.2' According to Dye, windows and objects thereby remain original form and location....This is pure improper hindsight.

9) The Office Action has provided no teaching or suggestion in Dye or elsewhere in the art to modify Dye as proposed by the Office Action, and fails to recognize that the proposed modification will still not yield Applicants' claimed subject matter....Applicants hereby request the Examiner provide support for an understanding of decoupling the input refresh rate from the output refresh rate as known in the art at the time of the invention in order to provide a smoother and more reliable display system.

10) Dye also fails to address "tearing"-the torn appearance of the portions of two separate frames, which is the type of problem addressed by Applicants' disclosed embodiment of decoupling recited in claim 1.

Examiner's Response

1) Dye discloses a video/graphics control which performs pointer-based display list video refresh operation. In Fig.2A, Dye discloses a system which includes the Interactive media controller 140, busses PCI and USB, system memory 110, and display 142. The detailed circuitry of the Controller 140 is shown in Figs. 5 and 6. As can be seen from Fig.6, a local bus, HD_bus, is coupled to the data Fifo 205 and another bus, Dbus2, couples the HD_bus to the fifo 205 with memory controllers 221/22 and other components of the controller (IMC 140). And whether Dye calls the HD_bus local bus or not, the function of HD_bus is, as can be seen from Fig.6 which is part of the disclosure of the Dye reference, the bus is a local bus. The So, Applicant's argument that the examiner is picking and choosing from different embodiments (presumably from unrelated parts/embodiments) is inaccurate and unpersuasive.

2) see response to Part (1).

3) the limitation in c) should have been "Digital television interface for receiving incoming digital TV data" which is met by Host I/F 202, fig. 6. The Examiner regrets the confusion. However, the rejection still remains.

4) The local bus interface for transmitting outgoing digital television data over the local bus is met by HD_ bus 207 and D_bus 2. Although the HD_bust 207 and Dbus1 and Dbus2 are labeled separately, the system clearly show an interface bus system for

transporting or transferring data from the command fifo 205, Execution unit 231, and RAM 232 to all other components. Further, please note that Fig. 6 shows the detailed circuitry of IMC 140 which is shown to couple with the PCI and USB busses in fig. 2b. The argument that the PCI and USB busses are not shown on Fig.6 makes not sense, because Fig.6 as mentioned above shows detailed circuitry of IMC 140. Thus, the argument PCI bus is not shown in Fig.6 and therefore the interface HD_bus cannot be a local bus transferring data etc. is unpersuasive, to say the least.

5) Dye discloses that FIG. 1B illustrates a television system which includes the IMC system and method of the present invention. In FIG. 1B, the television system 53 includes a display screen 59. The television system also preferably includes a set top box 57 which couples through a cable, such as a fiber optic cable or coaxial cable, for receiving video images for display on the television screen 59. The IMC of the present invention may be comprised in the television system unit 53 and/or may be comprised in the set top box 57. In other words, the IMC may be comprised in the set top box 57, or the IMC of the present invention may be integrated into the television, wherein the set top box 57 is optionally not included. The television system 53 is preferably a digital television. Alternatively, the television 53 is an analog television, wherein the set top box 57 operates to receive and/or store digital video data and provide analog video signals to the analog television. The television system 53 may also be adapted for interactive television or Internet applications, e.g., WebTV. In this case, the set top box includes a return path, such as a POTS telephone, ISDN, or DSL connection, for return

data." (col. 8, lines 14-35) therefore, the argument that the system of Dye does not process a digital television signal is false/inaccurate to say the least.

6) See rejection above.

7) Johnson doesn't merely mention *digital television system*. Johnson discloses or teaches that "In accordance with a further aspect of the present invention, there is provided a ***digital television system***." (col. 2, lines 55-56) If Applicant denies there is no disclosure here, then there is nothing the Examiner can do except to refer the applicant again to the passage where Johnson teaches a digital television system. The graphics/video subsystem 116 is shown in Fig.3 which is connected to the PC with a PCI bus 108 (col. 6, lines 21-26). The argument that Johnson does not disclose a digital television/local bus interface bus logic is again unpersuasive.

8) see new grounds for rejection of claim 1 (a) and (b);

9) Although Dye does not use the term Decoupled or separated or disengaged, Dye nevertheless teaches that "the pointer-based display list method of the present invention also allows screen refresh rate edge anti-aliasing and filtering method to be applied to video data on the fly as data is being refreshed on the screen. As discussed above, data is read from the system memory according to the current display refresh list, which is continually updated as screen changes occur." (col. 5, lines 50-55) Thus, the refresh rate of the incoming data and the refresh rate of the outgoing data would be different

because data is read from the system memory according to the current display refresh list, which is continually updated as screen changes occur. [emphasis added]

10) The applicant is arguing something that is not found in the claims. The claim does not recite "tearing- the torn appearance of the portions of tow separate frames". Thus, argument about what the application is about does nothing to change the rejection because the claims do not recite "tearing."

Allowable Subject Matter

6. Claims **48-52** are allowable over the prior art.

7. Claims **44** and **45** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a method for transferring digital television data in a system having a first frame buffer and a second frame buffer comprising: wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed, as in claim **44**; and wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device, as in claim **45**;

A memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital

television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device, as in claim **48**.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Kato et al., U.S. Patent No. 5,801,705 discloses a graphic display unit for implementing multiple frame buffer stereoscopic or blinking display.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-HELP.

Paulos Natnael PMN
December 26, 2003

JOHN MILLER
SUPERVISORY PATENT EXAMINER
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